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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO
09/881,226	06/12/2001	Roger May	015114-053300US	7601
26059	7590 02/09/2005		EXAMINER	
TOWNSENI	AND TOWNSEND	LI, ZHUO H		
TWO EMBAR	RCADERO CENTER			
8TH FLOOR			ART UNIT	PAPER NUMBER
SAN FRANCISCO, CA 94111-3834			2186	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
	09/881,226	MAY ET AL.				
Office Action Summary	Examiner	Art Unit				
	Zhuo H Li	2186				
The MAILING DATE of this communication a		correspondence address				
A SHORTENED STATUTORY PERIOD FOR REP THE MAILING DATE OF THIS COMMUNICATION - Extensions of time may be available under the provisions of 37 CFR after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a relif NO period for reply is specified above, the maximum statutory perior. - Failure to reply within the set or extended period for reply will, by state Any reply received by the Office later than three months after the mail earned patent term adjustment. See 37 CFR 1.704(b).	1. 1.136(a). In no event, however, may a reply be tileply within the statutory minimum of thirty (30) daily will apply and will expire SIX (6) MONTHS from the cause the application to become ABANDON	imely filed sys will be considered timely. In the mailing date of this communication. ED (35 U.S.C. § 133).				
Status						
1) Responsive to communication(s) filed on 22	November 2004.					
2a) This action is FINAL . 2b) ⊠ Th	nis action is non-final.					
	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
Disposition of Claims						
4) ☐ Claim(s) 1-12 and 46-53 is/are pending in the 4a) Of the above claim(s) is/are withdr 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 1-12 and 46-53 is/are rejected. 7) ☐ Claim(s) is/are objected to. 8) ☐ Claim(s) are subject to restriction and are	rawn from consideration.					
Application Papers						
9) ☐ The specification is objected to by the Examir 10) ☑ The drawing(s) filed on 16 November 2004 is. Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct 11) ☐ The oath or declaration is objected to by the Best State of the	/are: a)⊠ accepted or b)⊡ object te drawing(s) be held in abeyance. Se ection is required if the drawing(s) is ob	ee 37 CFR 1.85(a). Djected to. See 37 CFR 1.121(d).				
Priority under 35 U.S.C. § 119						
 12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of: 1. Certified copies of the priority documents. 2. Certified copies of the priority documents. 3. Copies of the certified copies of the priority documents. * See the attached detailed Office action for a list. 	nts have been received. nts have been received in Applicat iority documents have been receiv au (PCT Rule 17.2(a)).	ion No ed in this National Stage				
Attachment(s)						
 Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PTO-948) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08 Paper No(s)/Mail Date 	4) Interview Summary Paper No(s)/Mail D 8) 5) Notice of Informal I 6) Other:					

DETAILED ACTION

Response to Amendment

1. This Office action is in response to the amendment filed 11/22/2004.

Drawings

2. The drawings were received on 11/16/2004. These drawings are acceptable.

Accordingly, claims 13-45 are cancelled and claims 1-12 and 46-53 are pending for examination.

Claim Objections

3. Claim 46 is objected to because of the following informalities: claim 46, line 2, the second occurrence "when the" should be deleted. Appropriate correction is required.

Claim Rejections - 35 USC § 103

- 4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

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the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-4, 7-10, 46-51 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nojima (US PAT. 6,246,634) in view of Sugita (US PAT. 5,276,842).

Regarding claim 1, Nojima discloses a programmable logic integrated circuit (30, figure 1) comprising a programmable logic portion (60, figure 1), and an embedded processor portion and comprising a processor (i.e., 54, figure 1) and a memory block (i.e., 14, figure 1) coupled to the processor and comprising a memory having a first port and the second port (col. 2 line 13through col. 4 line 60). Nojima differs from the claimed invention in not specifically teaching the memory block comprising an arbiter coupled to the first port and the second port, wherein the arbiter arbitrates access to the memory by the first port and the second port. However, Sugita teaches a memory block comprising dual port memory (50, figure 10) and an arbiter coupled to a first port and a second port for arbitrating access to the memory by the first port and the second port in order to avoid access conflict to an address location (col. 2 lines 38-47 and col. 7 line 34 through col. 8 line 39). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Hardwood in having the memory block comprising the arbiter coupled to the first port and the second port, wherein the arbiter arbitrates access to the memory by the first port and the second port, as per teaching of Sugita, because it prevents access conflicts to an address location so that it prevents wrong data from being stored or retrieved.

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Regarding claim 2, Nojima discloses the memory being a dual port SRAM (col. 2 lines 26-29).

Regarding claim 3, Nojima discloses the programmable logi portion comprising a plurality of logic elements, programmably configurable to implement user-defined combinatorial or registered logic function (col. 3 lines 11-34).

Regarding claim 4, Nojima discloses the programmable logic portion comprising a plurality of horizontal and vertical interconnect lines programmably coupled to the plurality of logic elements (figure 1).

Regarding claim 7, Nojima discloses a programmable logic integrated circuit (30, figure 1) comprising a programmable logic portion (60, figure 1) having a plurality of logic elements, programmably configurable to implement user defined combinational or registered logic functions, and an embedded processor portion and comprising a processor (i.e., 54, figure 1) and a memory block (i.e., 14, figure 1) coupled to the processor and comprising a first plurality of memory cells for storing data and a second plurality of memory cells for storing data, a first port coupled to the first and second plurality of memory cells and a second port coupled to the first and second plurality of memory cells (col. 2 line 13through col. 4 line 60). Nojima differs from the claimed invention in not specifically teaching the memory block comprising an arbiter coupled to the first port and the second port, wherein the arbiter prevents the first port from accessing the first plurality of memory cells when the second port is accessing a subset of the first plurality of memory cells and the arbiter allows the first port to access the second plurality of memory cells when the second port is accessing the first plurality of memory cells when the second port is access the second plurality of memory cells when the second port is accessing the first plurality of memory cells. However, Sugita teaches a memory block comprising dual port memory (50, figure 10) and

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an arbiter coupled to a first port and a second port for arbitrating access to the memory by the first port and the second port in order to avoid access conflict to an address location (col. 2 lines 38-47 and col. 7 line 34 through col. 8 line 39). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Hardwood in having the memory block comprising the arbiter coupled to the first port and the second port, wherein the arbiter prevents the first port from accessing the first plurality of memory cells when the second port is accessing a subset of the first plurality of memory cells and the arbiter allows the first port to access the second plurality of memory cells when the second port is accessing the subset of the first plurality of memory cells, as per teaching of Sugita, because it prevents access conflicts to an address location so that it prevents wrong data from being stored or retrieved.

Regarding claim 8, Nojima discloses the first plurality of memory cells and the second plurality of memory cells being defined by a user programmable lock register (col. 2 lines 42-65).

Regarding claim 9, Nojima discloses the first and second plurality of memory cells comprising a portion of dual-port SRAM (figure 1 and col. 2 lines 23-29).

Regarding claim 10, the limitations of the claim are rejected as the same reasons set forth in claim 4.

Regarding claim 46, Sugita teaches the arbiter allows the first port to access the first plurality of memory cells when the second port is accessing a subset of the second plurality of memory cells and the arbiter allows the first port to access the second plurality of memory cells when the second port is accessing the subset of the first plurality of memory cells (col. 8 line 1 through col. 9 line 56).

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Regarding claim 47, the limitations of the claim are rejected as the same reasons set forth in claim 7.

Regarding claim 48, the limitations of the claim are rejected as the same reasons set forth in claim 46.

Regarding claim 49, the limitations of the claim are rejected as the same reasons set forth in claim 3.

Regarding claim 50, Nojima discloses the integrated circuit further comprising an embedded processor portion coupled to the programmable logic portion and comprising a processor and the memory block (figure 1).

Regarding claim 51, the limitations of the claim are rejected as the same reasons set forth in claim 8.

Regarding claim 53, Nojima discloses the integrated circuit being a programmable logic device (col. 2 lines 15-29).

6. Claims 5-6, 11-12 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nojima (US PAT. 6,246,634) in view of Sugita (US PAT. 5,276,842) as applied in claims above, and further in view of Phelan et al. (US PAT. 6,499,089 hereinafter Phelan).

Regarding claims 5-6, the combination of Nojima and Sugita differs from the claimed invention in not specifically teaching the second port, as well as the first port, being configurable in width and depth. However, Phelan teaches an integrated circuit having both first and second ports being configurable in width and depth (col. 2 lines 11-14) in order to allow different width of data to be read out from the memory based upon the requirements of different processors,

thereby improving memory versatility. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Nojima and Sugita in having the second port, as well as the first port, being configurable in width and depth, as per teaching of Phelan, in order to allow different width of data to be read out from the memory based upon the requirements of different processors, thereby improving memory versatility.

Regarding claims 11-12, the limitations of the claims are rejected as the same reasons set forth in claims 5-6.

Regarding claim 52, the limitations of the claim are rejected as the same reasons set forth in claims 5-6.

Response to Arguments

7. Applicant's arguments with respect to claims 1-12 and 46-53 have been considered but are most in view of the new ground(s) of rejection.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Harwood, III (US PAT. 5,644,756) discloses an integrated circuit data processor with selectable routing of data access (abstract). Rao (US PAT. 5,953,738) discloses a memory being fabricated as a single integrated circuit chip including an array of memory cells and circuitry for accessing selected memory cells (col. 3 line 49 through col. 4 line 62). Van Hook et al. (US

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PAT. 6,567,426) disclose a method for sharing a data memory among a plurality of processor in

a computer system (abstract).

9. Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Zhuo H. Li whose telephone number is 571-272-4183. The

examiner can normally be reached on Tue-Fri 8:30 AM-6:00 PM, and alternate Monday 8:30

AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

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system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zhuo H. Li Patent Examiner